REMARKS

After entry of this amendment, claims 1, 3-11, and 13-25 are pending. In the present Office Action, claims 1-2, 11-12, and 20-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Frederick, Jr. et al., U.S. Patent No. 6,178,497 ("Frederick"). Claims 3-10 and 13-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Frederick in view of Roy, U.S. Patent No. 6,785,802 ("Roy"). Applicants respectfully traverse these rejections and request reconsideration.

Claim 1 recites a combination of features including: "a plurality of age vectors, each of the plurality of age vectors corresponding to one or more of the plurality of entries", citing Frederick's age "vector" A_i. Applicants respectfully disagree that Frederick teaches a plurality of age vectors, and disagree that A_i is a vector. It is true that Frederick sometimes refers to A_i as a vector, but Applicants respectfully submit that this is sloppy use of language in Frederick. Frederick provides a truth table (table 2, column 6) which specifies A_i as a bit (either zero or one for all combinations of T_i, V_i, and I_{i-1}). Accordingly, A_i is a scalar value, not a vector. A vector, as used in the digital arts, is a multi-valued entity (e.g. a vector of bits, in some embodiments). Furthermore, Frederick refers to other values as "vectors" and also as single values (e.g. T_i, V_i, and I_{i-1}) Accordingly, Frederick teaches a single age vector A, whose values are the bits A_i for each entry in Frederick's queue.

Furthermore, claim 1 recites "the control circuit is configured, responsive to data being provided to the buffer to be written to at least a first entry of the plurality of entries, to generate a first age vector of the plurality of age vectors, the first age vector corresponding to at least the first entry". Frederick does not explicitly state when he generates his age bits A_i. Thus, Frederick fails to anticipate the above highlighted features. Additionally, Frederick defines his age bits A_i as being dependent on the tail vector bits T_i, which change over time. This definition implies that the age bits are generated at the time of reading Frederick's queue, not at the writing of the queue.

For at least the above stated reasons, Applicants submit that Frederick's alleged

anticipation of claim 1 is not supported by the art, and thus the rejection must be rescinded. Claim 11 recites a combination of features including: "generating a first age vector of a plurality of age vectors responsive to receiving the data, each of the plurality of age vectors corresponding to one or more of the plurality of entries, the first age vector corresponding to at least the first entry". The same teachings of Frederick highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 11. Applicants respectfully submit that Frederick does not anticipate the above features of claim 11, either, and thus the rejection of claim 11 must be rescinded. Claim 20 recites a combination of features including: "a plurality of age vectors, each of the plurality of age vectors corresponding to one or more of the plurality of entries; and a control circuit ... configured, responsive to data being provided to the buffer to be written to at least a first entry of the plurality of entries, to generate a first age vector of the plurality of age vectors, the first age vector corresponding to at least the first entry". The same teachings of Frederick highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 20. Applicants respectfully submit that Frederick does not anticipate the above features of claim 20, either, and thus the rejection of claim 20 must be rescinded.

Claims 3-10 and 24 (dependent from claim 1), claims 13-19 and 25 (dependent from claim 11) and claims 21-23 (dependent from claim 20) are believed to be in condition for allowance at least via their dependence on claims 1, 11, and 20. Additionally, each of the dependent claims recites additional combinations of features not taught or suggested in Frederick, or in Frederick in view of Roy.

For example, the Office Action alleges that claims 21-23 are anticipated by Frederick, citing Fig. 1 and its description. Applicants respectfully disagree. The only buffer described in Frederick with respect to Fig. 1 appears to be the rename buffers 34 (see Fig. 1 and its description, col. 2, line 41-col. 4, line 21). With respect to Fig. 2, Frederick states that his queue 201 may be used in any queue in processor 10, but no queues appear to be described with respect to Fig. 1 (again, see col. 2, line 41-col. 4, line 21 of Frederick). To anticipate a claim, a single prior art reference must teach or suggest

EACH and EVERY feature of the claim. Applicants respectfully submit that Frederick fails to teach "at least one circular buffer implemented in a scheduler, the data stored in each entry comprising operations to be executed by one or more execution cores in the processor" as recited in claim 21; "at least one circular buffer implemented in a retire queue" as recited in claim 22; and "at least one circular buffer implemented as a load/store buffer storing load/store operations" as recited in claim 23.

The Office Action further alleges, with regard to claims 4 and 13, that the recited features would be obvious. The Office Action admits that neither Frederick nor Roy teaches the recited features, but concludes that these features would be obvious. Applicants note that, to form a *prima facie* case of obviousness for a claim, EACH and EVERY feature of a claim must be taught or suggested in the cited art. Neither Frederick nor Roy teaches the features of claim 4 and 13 (as the Office Action states), and no evidence has been provided to indicate that such features are in the prior art.

Furthermore, the Office Action states that grouping entries into non-overlapping groups would be obvious so a greater amount of older data would be processed per instruction cycle utilizing the superscalar processors taught by Frederick and Roy. Applicants respectfully disagree with this reasoning. Superscalar processors typically use out of order execution to identify disparate instructions for concurrent execution, to take advantage of the multiple execution resources provided by the processor. For example, instructions of different types are often separately scheduled to the various execution unit types. See, e.g., Roy, col. 4, lines 14-32. Thus, no grouping of entries would be possible. For at least the above reasons, Applicants respectfully submit that a *prima facie* case of obviousness has not been proven for claims 4 and 13.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-90500/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

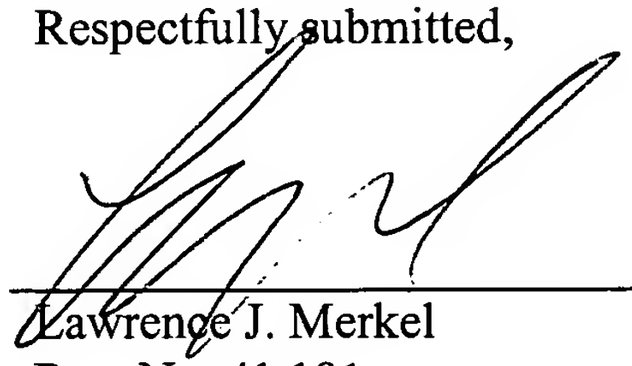
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 11/2/05